What is claimed is:

1. An electronic circuit system comprising:

at least three macro circuits each including a logic circuit and a memory circuit, and having a plurality of input terminals and a plurality of output terminals; and

a plurality of signal lines for connecting the macro circuits to one another into a loop to transmit signals in a single specified direction through the loop in synchronization with a clock signal,

each of the macro circuits receiving the signals at the input terminals thereof, accepting the received signals if the received signals are destined thereto, and transferring the received signals to the output terminals thereof without accepting the received signals if the received signals are not destined thereto.

2. An electronic circuit system as claimed in claim 1, wherein any one of the macro circuits that accepted the received signals clears the received signals and transmits the cleared signals from the output terminals thereof.

3. An electronic circuit system as claimed in claim 1, wherein any one of the macro circuits, which are unavailable for accepting the received signals even if the received signals are destined thereto, transfers the received signals as they are, without accepting them, to the output terminals thereof.

4. An electronic circuit system as claimed in claim 1, wherein:

each of the macro circuits has a core and a station circuit; and

the station circuit selectively carries out at least the outputting of signals to the output terminals according to a request from the core, the accepting, clearing, and transferring to the output terminals of received signals, and the transferring of received signals as they are, without accepting them, to

the output terminals.

5. An electronic circuit system as claimed in claim 4, wherein:

the station circuit has an input circuit, an output circuit, and a station interface;

the input circuit fatches signals received by the input terminals in response to the clock signal;

the output circuit fetches signals from the station interface and transfers the signals to the output terminals in response to the clock signal; and

the station interface selectively carries out at least the outputting of signals to the output circuit according to a request from the core, the accepting, clearing, and transferring to the output circuit of signals received by the input circuit, and the transferring of signals received by the input circuit as they are, without accepting them, to the output circuit.

6. An electronic circuit system as claimed in claim 1, wherein the macro circuits include an I/O circuit for transmitting signals to an external circuit.

7. An electronic circuit system as claimed in claim 1, wherein the macro circuits include an I/O circuit for receiving signals from an external circuit.

8. An electronic circuit system as claimed in claim 1, wherein the macro circuits include an I/O circuit for communicating signals with an external circuit.

9. An electronic circuit system as claimed in claim 1, wherein each memory circuit among the macro circuits provides a busy signal when continuously accessed by another macro circuit, so that any other macro circuit that intends to access the memory circuit is put in a wait state in response to the busy signal.

10. An electronic circuit system as claimed in claim 1, wherein each memory circuit among the macro circuits provides a busy signal when continuously accessed by an external circuit, so that any other macro

circuit that intends to access the memory circuit is put in a wait state in response to the busy signal.

11. An electronic circuit system as claimed in claim 1, further comprising a macro circuit that is out of the loop.

12. An electronic circuit system as claimed in claim 1, wherein:

the signal lines include command-related lines for transmitting command-related signal and data-related lines for transmitting data-related signals;

the command-related lines include a command flag line for transmitting a command flag signal that contains a command originator and a command destination, a command line for transmitting a command signal, and an address line for transmitting an address signal indicating an address in a macro circuit that is the command destination; and

the data-related lines include a data flag line for transmitting a data flag signal indicating a data destination and a data line for transmitting a data signal.

13. An electronic circuit system as claimed in claim 12, wherein the logic circuit transmits the following signals from the output terminals thereof when carrying out a read access to one of the memory circuits:

a command flag signal indicating a command originator and a command destination;

a command signal indicating a read command; and

an address signal indicating an address to access in the memory circuit.

14. An electronic circuit system as claimed in claim 12, wherein the logic circuit transmits the following signals from the output terminals thereof when carrying out a write access to one of the memory circuits:

a command flag signal indicating a command

originator and a command destination;

a command signal indicating a write command;

an address signal indicating an address to access in the memory circuit;

a data flag signal indicating a data destination; and

a data signal.

15. An electronic circuit system as claimed in claim 14, wherein the operation of the core of the logic circuit is stopped before the I/O circuit transfers command-related signals from an external circuit to the signal lines.

16. An electronic circuit system as claimed in claim 15, wherein the operation of the core of the logic circuit is stopped a predetermined number of clock cycles before the I/O circuit transfers command-related signals from an external circuit to the signal lines.

17. An electronic circuit system comprising:

a first macro circuit constituted by a logic circuit having a plurality of input terminals and a plurality of output terminals;

second to "n"th macro circuits (n being an integer lager than 3) each including a memory circuit but no logic circuit, and having a plurality of input terminals and a plurality of output terminals; and

a plurality of signal lines for connecting the first to "n"th macro circuits to one another into a half loop with the output terminals of the first macro circuit being at the start of the half loop and the input terminals of the first macro circuit at the end of the half loop, to transmit signals in a single specified direction through the half loop in synchronization with a clock signal,

the first macro circuit accepting signals received by the input terminals thereof if the received signals are destined for the first macro circuit,

each of the second to "n"th macro circuits accepting signals received by the input terminals thereof if the received signals are destined thereto and transmitting the received signals as they are from the output terminals thereof, without accepting the received signals, if the received signals are not destined thereto.

18. An electronic circuit system as claimed in claim 17, wherein:

each of the second to "n"th macro circuits has a core and a station circuit; and

the station circuit selectively carries out at least the outputting of signals to the output terminals according to a request from the core, the accepting, clearing, and transferring to the output terminals of received signals, and the transferring of received signals as they are, without accepting them, to the output terminals.

19. An electronic circuit system as claimed in claim 18, wherein:

the station circuit has an input circuit, an output circuit, and a station interface;

the input circuit fetches signals received by the input terminals in response to the clock signal;

the output circuit fetches signals from the station interface and transfers the signals to the output terminals in response to the clock signal; and

the station interface selectively carries out at least the outputting of signals to the output circuit according to a request from the core, the accepting, clearing, and transferring to the output circuit of signals received by the input circuit, and the transferring of signals received by the input circuit as they are, without accepting them, to the output circuit.

20. An electronic circuit system as claimed in claim 19, wherein each of the signal lines connects the adjacent macro circuit to each other through a latch

circuit for latching signals in synchronization with the clock signal.

21. An electronic circuit system as claimed in claim 17, wherein the second to "n"th macro circuits include not only the memory circuits, but also an I/O circuit for transmitting signals to an external circuit.

22. An electronic circuit system as claimed in claim 17, wherein the second to "n"th macro circuits include not only the memory circuits, but also an I/O circuit for receiving signals from an eternal circuit.

23. An electronic circuit system as claimed in claim 17, wherein the second to "n"th macro circuits include not only the memory circuits, but also an I/O circuit for communicating signals with an external circuit.

24. An electronic circuit system as claimed in claim 17, wherein:

the signal lines include command-related lines for transmitting command-related signals and data-related lines for transmitting data-related signals;

the command-related lines include a command flag line for transmitting a command flag signal that contains a command originator and a command destination, a command line for transmitting a command signal, and an address line for transmitting an address signal indicating an address in a macro circuit that is the command destination; and

the data-related lines include a data flag line for transmitting a data flag signal indicating a data destination and a data line for transmitting a data signal.

25. An electronic circuit system as claimed in claim 24, wherein the logic circuit transmits the following signals from the output terminals thereof when carrying out a read access to one of the memory circuits:

a command flag signal indicating a command originator and a command destination;

a command signal indicating a read command; and

an address signal indicating an address to access in the memory circuit.

26. An electronic circuit system as claimed in claim 24, wherein the logic circuit transmits the following signals from the output terminals thereof when carrying out a write access to one of the memory circuits:

a command flag signal indicating a command originator and a command destination;

a command signal indicating a write command;

an address signal indicating an address to access in the memory circuit;

a data flag signal indicating a data destination; and

a data signal.

27. An electronic circuit system as claimed in claim 26, wherein the operation of the core of the logic circuit is stopped before the I/O circuit transfers command-related signals from an external circuit to the signal lines.

28. An electronic circuit system as claimed in claim 27, wherein the operation of the core of the logic circuit is stopped a predetermined number of clock cycles before the I/O circuit transfers command-related signals from an external circuit to the signal lines.

29. An electronic circuit system comprising:

a plurality of external input terminals for receiving test signals;

first to "m-1"th macro circuits (m being an integer larger than 2) each having a plurality of input terminals and a plurality of output terminals for receiving and transmitting the test signals;

an "m"th macro circuit having input terminals for receiving the test signals; and

a plurality of signal lines for transmitting the test signals and connecting the external input terminals and the first to "m"th macro circuits to one another into a half loop with the external input terminals being at the start of the half loop and the input terminals of the "m"th macro circuit at the end of the half loop, to transmit the test signals in a single specified direction through the half loop in synchronization with a clock signal,

each of the first to "m-1"th macro circuits accepting the test signals received by the input terminals thereof if the test signals are destined thereto and transmitting the test signals from the output terminals thereof, without accepting the test signals, if the test signals are not destined thereto,

the "m"th macro circuit accepting the test signals received by the input terminals thereof if the test signals are destined thereto.

30. An electronic circuit system as claimed in claim 29, wherein the macro circuits are memory circuits.

31. An electronic circuit system as claimed in claim 29, wherein:

each of the macro circuits has a core and a station circuit; and

the station circuit selectively carries out at least the accepting of received signals and the transferring of the received signals to the output terminals.

32. An electronic circuit system as claimed in claim 31, wherein:

the station circuit has an input circuit, an output circuit, and a station interface;

the input circuit fetches signals received by the input terminals in response to the clock signal;

the output circuit fetches signals from the station interface and transfers the signals to the output terminals in response to the clock signal; and

the station interface selectively carries out at least the accepting of received signals and the transferring of the received signals to the output terminals.

33. An electronic circuit system as claimed in claim 29, wherein each of the signal lines connects the adjacent macro circuits to each other through a latch circuit for latching signals in synchronization with the clock signal.

34. A signal transmission method comprising the steps of:

connecting at least three macro circuits each having a plurality of input terminals and a plurality of output terminals to one another through signal lines to transmit signals in a single specified direction in synchronization with a clock signal; and

making each of the macro circuits accept signals received by the input terminals thereof if the received signals are destined thereto and transfer the received signals as they are, without accepting them, to the output terminals thereof if the received signals are not destined thereto.

35. A signal transmission method comprising the steps of:

connecting first to "n"th macro circuits (n being an integer larger than 3) each having a plurality of input terminals and a plurality of output terminals to one another through signal lines into a half loop, the first macro circuit being a logic circuit, each of the second to "n"th macro circuits including a memory circuit but no logic circuit and having a plurality of input terminals and a plurality of output terminals, the output terminals of the first macro circuit being at the start of the half loop, the input terminals of the first macro circuit being at the end of the half loop to transmit signals in a single specified direction through the half loop in synchronization with a clock signal;

making each of the second to "n"th macro circuits accept signals received by the input terminals thereof if the received signals are destined thereto and transmit the received signals from the output terminals thereof, without accepting the received signals, if the received signals are not destined thereto; and

making the first macro circuit accept signals received by the input terminals thereof if the received signals are destined thereto.

36. A signal transmission method comprising the steps of:

connecting a plurality of external input terminals for receiving test signals, first to "m-1"th macro circuits (m being an integer greater than 2) each having a plurality of input terminals and a plurality of output terminals for receiving and transmitting the test signals, and an "m"th macro circuit having a plurality of input terminals for receiving the test signals, to one another into a half loop through signal lines for transmitting the test signals, the external input terminals being at the start of the half loop, the input terminals of the "m"th macro circuit being at the end of the half loop to transmit the test signals in a single specified direction through the half loop in synchronization with a clock signal;

making each of the first to "m-1"th macro circuits accept the test signals received by the input terminals thereof if the test signals are destined thereto and transmitting the test signals from the output terminals thereof, without accepting the test signals, if the test signals are not destined thereto; and

making the "m"th macro circuit accept the test signals received by the input terminals thereof if the test signals are destined thereto.

37. A signal transmission method as claimed in claim 36, wherein the signal lines include an I/O circuit for receiving, from the outside, test signals for testing

the first to "m"th macro circuits.

38. A signal transmission method as claimed in claim 36, wherein the test signal lines include an I/O circuit for receiving, from the outside, test signals for testing memory circuits among the first to "m"th macro circuits.

39. A signal transmission method as claimed in claim 36, wherein the test signal lines include an I/O circuit for receiving, from the outside, test signals for testing logic circuits among the first to "m"th macro circuits.

40. A signal transmission method as claimed in claim 36, wherein the test signal lines include an I/O circuit and a built-in self-test circuit that generates test signals for testing the first to "m"th macro circuits according to signals entered into the I/O circuit.

09372156.081199

33